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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/010,343	12/05/2001	Visvamohan Yegnashankaran	072219-0261615 (P05089)	7286

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EXAMINER

ANDUJAR, LEONARDO

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 08/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/010,343

Applicant(s)

YEGNASHANKARAN ET AL.

Examiner

Leonardo Andújar

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 May 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 and 21-37 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 21, 22, 24, 25, 27-30 and 32 is/are rejected.
- 7) ☒ Claim(s) 23, 26, 31 and 33-37 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 May 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Acknowledgment

1. The amendment filed on 05/27/2003, paper no. 10, in response to the Office action mailed on 02/27/2003 has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-3 and 21-37.

Drawings

2. The proposed drawing corrections and/or the proposed substitute sheets of drawings, filed on 05/27/2003 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance. Also, the formal drawings filed on August 09, 2002 have not been received.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-3, 22, 24, 25, 28-30 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wark (US 6,399,416) in view of Wolf.

5. Regarding claim 1, Wark (see figure 2 attached to paper no. 9) shows an integrated circuit comprising:

➤ A first die 26 having:

- a. A substrate with an electrical circuit (col. 4/lis. 27-35);
- b. A plurality of first bonding pads 26a;
- c. A plurality of second bonding pads 26b;

➤ A second die 32;

- a. A micro electro-mechanical structure having inductance;
- b. A plurality of third bonding pads 32a connected to the micro electro-mechanical structure;
- c. A plurality of connectors 32b electrically connected to the second bonding pads and the third bonding pad;

6. Wark does not explicitly teach that the IC chip 26 includes interconnects formed on the substrate and electrically connected to the electrical circuit, and a passivation layer. Nonetheless, it is well known in the art that IC chips include interconnects on the semiconductor substrate as well as bonding pads formed on a passivation layer. Wolf teaches that metal interconnections (one or more level) are formed on the substrate to interconnect circuit elements and to carry large amounts of supply current. Moreover, passivation layers are used to protect the device from contaminants, moisture and scratches (pages 826-829). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form interconnects on Wark's substrate in order to interconnect the circuit elements as taught by Wolf. Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the plurality of first and second bonding pads disclosed by Wark on a passivation layer in

order to protect the device from contaminants, moisture and scratches as taught by Wolf.

7. Regarding claims 2 and 32, Wark discloses a package 12 having a plurality of fourth bonding pads, a plurality of circuit boards connectors, and internal routing (fig. 3b, col. 4/lis. 46-54). Also, Wark discloses a plurality of wires 26c connected to the first bonding pads and the fourth bonding pads.

8. Regarding claim 3, Wark discloses that the second die include a capacitive micro electromechanical structure that has capacitance (col. 4/lis. 27-35, col. 5/lis. 20-27).

9. Regarding claims 22 and 25, Wark in view of Wolf teaches that the passivation layer has a top surface, a center region of the top surface, and a peripheral region of the top surface that surrounds the center region. Also, the plurality of first bonding pads are formed on the passivation layer only in the peripheral region and the plurality of second bonding pads are formed on the passivation layer only in the center region.

10. Regarding claim 24, Wark shows that the package has a top surface and a bottom surface, the plurality of fourth bonding pads 36 are located on the top surface, and a plurality of a circuit board connector 38 are located at the bottom surface (3B).

11. Regarding claim 28, Wark discloses that the second die includes a micro-electromechanical structure.

12. Regarding claim 29 and 30, Wark discloses that the micro-electromechanical structure 26 is a DRAM IC die (col. 4/lis. 30-31). Any DRAM IC die inherently has capacitance and inductance

13. Claims 21 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wark (US 6,399,416) in view of Wolf further in view of Harper.

14. Regarding claims 21 and 27, Wark in view of Wolf discloses most aspects of the instant invention including plurality of connectors. Wark in view of Wolf does not show that the connectors include a solder. Nonetheless, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen arrangement or upon another variable recited in a claim, the applicant must show that the chosen arrangements are critical. In *re* Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990). Furthermore, the selection of the connection type such as pin, solder ball, flip chip, wire bonding, etc is a matter of design choice since its depend on design variable like the type of supporting substrate, available connection area and electrical performance. Note that obvious design choice limitations are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *in re* Leshin, 125 USPQ 416. For example, Harper teaches that the large cross-section and the inherent shorter length of solder bumps provide a significant reduction in lead inductance. Also, this type of interconnection provides an excellent electrical performance (pg. 6.71-73). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a solder ball connection make the plurality of connectors disclosed by Wark in view of Wolf in order to improve device electrical performance and to reduce the pin inductance as taught by Harper.

Allowable Subject Matter

15. Claims 23, 26, 31 and 33-37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

16. Applicant's arguments filed 05/27/2003 have been fully considered but they are not persuasive.

17. Applicant argues that Wark does not teach or suggest that the die 32 includes a micro electromechanical structure that has an inductance. Nonetheless, Wark teaches that one or more IC dies 32 are stacked over the IC die 26 (col. 5/lis. 20-28). Note that any IC chip such as a DRAM IC inherently has some degree of inductance. Furthermore, a stack arrangement of IC chips inherently has inductance.

18. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a first die that performs a first function, a second die that performs a second function and a third die that performs a third function) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final

action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

20. Papers related to this application may be submitted directly to Art Unit 2826 by facsimile transmission. Papers should be faxed to Art Unit 2826 via the Art Unit 2826 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2826 Fax Center number is **(703) 308-7722** or **-7724**. The Art Unit 2826 Fax Center is to be used only for papers related to Art Unit 2826 applications.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Leonardo Andújar** at **(703) 308-0080** and between the hours of 9:00 AM to 7:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Leonardo.Andujar@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn, can be reached on (703) 308-6601.

22. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 305-3900**.

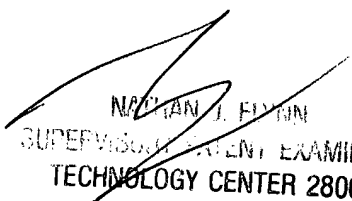
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23. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass (es): 257/777	08/03
Other Documentation:	
Electronic Database(s): East (USPAT, US PGPUB, JPO, EPO, Derwent, IBM TDB)	08/03

Leonardo Andújar

Patent Examiner Art Unit 2826

LA
8/10/03

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